

# **Graphene Field-Effect Transistor (GFET) Chips**

METALS ◆ INORGANICS ◆ ORGANOMETALLICS ◆ CATALYSTS ◆ LIGANDS ◆ NANOMATERIALS ◆ CUSTOM SYNTHESIS ◆ cGMP FACILITIES

GFET chips provide researchers with direct access to the latest graphene devices. This promotes application-driven research without a need to construct GFETs from scratch. Each chip provides 36 individual GFETs distributed in different patterns - **06-2555**: Grid pattern, **06-2560**: Quadrant pattern.

06-2555: Graphene Field-Effect Transistor (GFET) Chip - Grid pattern

06-2560: Graphene Field-Effect Transistor (GFET) Chip - Quadrant pattern

### **FEATURES:**

- Devices not encapsulated ready for your functionalization
- Perfect platform device for new sensor research and development
- 36 individual GFETs per chip
- Mobilities typically in excess of 1000 cm2/V.s

#### **APPLICATIONS:**

- Graphene device research
- Chemical sensors
- Biosensors
- Bioelectronics
- Magnetic sensors
- Photodetectors

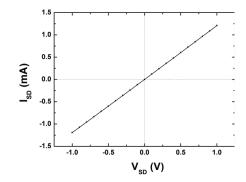
#### **TYPICAL SPECIFICATIONS:**

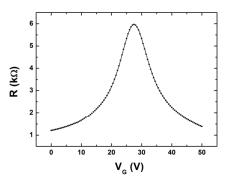
Chip dimensions	10 mm x 10 mm
Chip thickness	675 μm
Number of GFETs per chip	36
Gate Oxide thickness	90 nm
Gate Oxide material	SiO <sub>2</sub>
Resistivity of substrate	1-10 Ω.cm
Metallization	Nickel/Aluminium 140 nm
Graphene field-effect mobility	>1000 cm <sup>2</sup> /V.s
Residual charge carrier density	<2 x 10 <sup>12</sup> cm <sup>-2</sup>
Dirac point	10-40 V
Yield	>75 %

## **DEVICE CROSS-SECTION:**



#### **TYPICAL CHARACTERISTICS:**



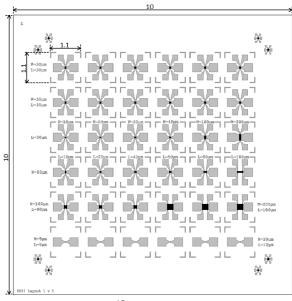


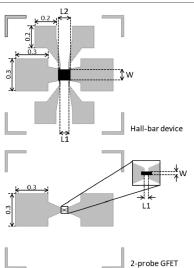
## **ABSOLUTE MAXIMUM RATINGS:**

Maximum gate-source voltage	± 50 V
Maximum temperature rating	150 °C
Maximum drain-source current density	10 <sup>7</sup> A.cm <sup>-2</sup>

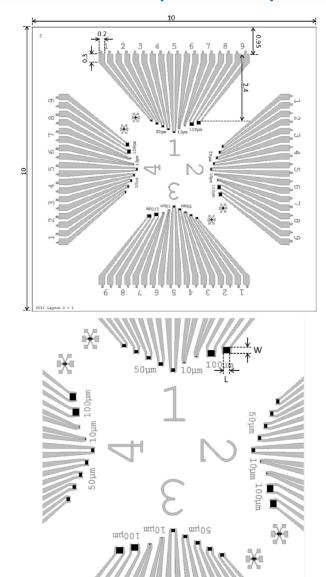
Output curve (left) and transfer curve measured at source-drain voltage of 20mV (right), measured at room temperature and vacuum conditions on a device with  $W=L=50~\mu m$ .

# 06-2555: GFET Chip - Grid pattern





# 06-2560: GFET Chip - Quadrant pattern



## **CHANNEL GEOMETRIES**

Description	<b>W</b> (μm)	<b>L1</b> (μm)	<b>L2</b> (μm)	Quantity
Standard	50	30	50	12
	10			1
	20			1
Vom in a Midth	30	30	50	1
Varying Width	40	30		1
	100			1
	200			1
Largo Causto	100	80 180	100	3
Large Square	200		200	3
		10	30	1
		20	40	1
Mar to describ	Varying length 50	40	60	1
varying length		50	70	1
		80	100	1
		180	200	1
Small 2-probe	5	5		3
	10	10		3

Device number	<b>W</b> (μm)	<b>L</b> (μm)
1	50	50
2		
3		
4		
5		
6	10	10
7		
8	100	100
9	100	100

## **Basic Handling Instructions**

The graphene used in our GFETs is high-quality monolayer CVD graphene and highly prone to damage by external factors. To maintain the quality of your devices, we recommend taking the following precautions:

- Be careful when handling the GFET chip that tweezers do not make contact with the device area. Metallic tweezers should be avoided, as they can damage/scratch the chip edges/surfaces.
- Treat the devices as sensitive electronic devices and take precautions against electrostatic discharge.
- Ideally store in inert atmosphere or under vacuum in order to minimize adsorption of unknown species from the ambient air.
- Do not ultrasonicate the GFET dies.
- Do not apply any plasma treatment to the GFET dies.
- Do not subject the GFET dies to strongly oxidizing reagents.

## **Doping-reduction treatment**

Graphene on SiO<sub>2</sub> is often p-doped after exposure to air due to the adsorption of water molecules and other adsorbates with the effect that the Dirac point is shifter to positive gate voltages and can cause the Dirac voltage to be located out of the recommended gate voltage range. In addition, a large hysteresis is observed between the forward and backward sweeps of a transfer curve.

Immersing the GFET chip in acetone for at least 12h reduces doping. After that the chip should be immediately rinsed with IPA, properly dried with an Ar or  $N_2$  gun, and shortly introduced into the measurement equipment. In order to preserve the effectivity of this treatment, electrical characterization should be carried out in inert atmosphere or vacuum.

In addition, storage of the chips in a low humidity environment (N<sub>2</sub> cabinet, desiccator, or vacuum) is highly recommended.

## **Typical Measurement Configurations**

#### 2-probe devices (electrical measurements that can be performed on the different devices in both 06-2555 & 06-2560)

These devices allow field-effect measurements by simultaneously applying two voltages:

- Source-drained voltage (V<sub>SD</sub>): applied between the two probes (source and drain), while one of them is grounded (see Figure 1a). V<sub>SD</sub> enables the transport of charge carriers through the graphene channel, with an associated source-drain current (I<sub>SD</sub>). V<sub>SD</sub> can be varied in order to ge the desired I<sub>SD</sub> outcome (see Figure 1b).
- Gate voltage (V<sub>G</sub>): applied to the Si on the substrate. V<sub>G</sub> creates an electric field on the graphene channel, modulating the conductivity of graphene (see Figure 1c).

The Si can be contacted either from the top surface by scratching the 90nm-thick  $SiO_2$  with a diamond pen in one of the chip corners; or alternatively from the underside of the chip, for instance using a proble station chuck.

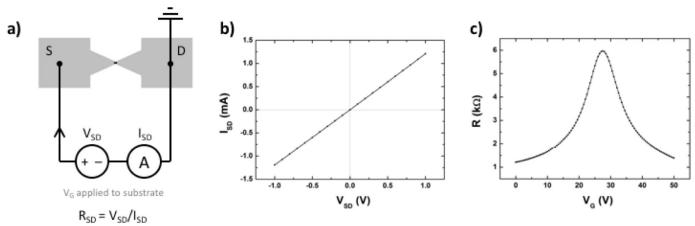


Figure 1: a) Scheme of the 2-probe device, with the corresponding electrical measurement configuration.

- b) Typical output measured at room temperature and vacuum conditions.
- c) Typical transfer curve measured at  $V_{\rm SD}$ =20mV (right), measured at the same conditions as in 1b.

## **Typical Measurement Configurations (continued)**

## Hall Bars (electrical measurements that can be performed on the different devices in 06-2555 only)

#### Field-effect measurement

A common modification on the 2-probe GFET measurement is to apply a source-drain voltage between two outer contacts, measure the current between those two contacts but additionally measure the voltage directly across the graphene channel using two additional inner contacts, V12 (see Figure 2). The benefit of this is that the resistance of the graphene channel alone can be measured without including any voltage drops at the graphene-metal interfaces.

The graphene-metal interface resistance does depend on VG but not in the same way as the graphene channel resistance therefore measuring the graphene channel resistance directly in the 4-probe measurement configuration can achieve greater sensitivity to applied gate fields or surface charge changes.

The resistivity of graphene is usually expressed per thickness unit, i.e. the so-called sheet resistance:

 $R_S = R_{CH} \frac{W}{L1},$ 

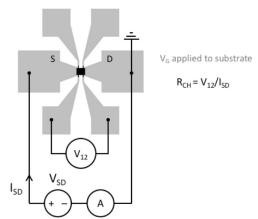


Figure 2: Scheme of the 4-probe measurement in a Hall bar device, with the corresponding electrical measurement configuration.

being RCH the resistance of the graphene channel, and W and L1 the width and inner length of the graphene channel, respectively. The field-effect mobility (µFE) can be calculated by using the following equation:

$$\mu_{FE} = g \cdot \frac{1}{C_{SiO2}},$$

where:

- g =  $d\delta/dV_G$  is the transconductance, being  $\delta=1/R_S$ ,
- C<sub>SiO2</sub> is the capacitance per unit area of the 90 nm-thick SiO<sub>2</sub> dielectric.

 $\mu_{\text{FE}}$  is usually calculated using the maximum transconductance.

The field-effect charge carrier density  $(n_{FF})$  is calculated as follows:

$$n_{FE} = \mu_{FE} \cdot R_S / e$$

In order to extract the residual carrier concentration  $n_0$ , i.e. the charge carrier density at the Dirac point, we can use the following expression:

$$n_{FE}=\sqrt{n_0^2+n_G^2},$$

where n<sub>G</sub> is the gate-induced charge carrier density, which is calculated from the following equation:

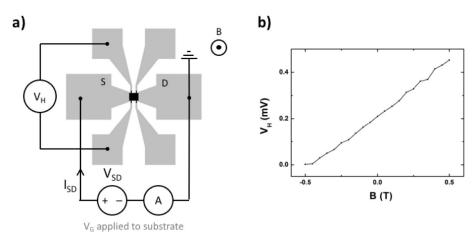
$$V_G - V_D = \frac{e}{C_{SiG2}} n_G + \frac{\hbar v_F \sqrt{\pi \cdot n_G}}{e},$$

where  $V_{\scriptscriptstyle D}$  is the Dirac voltage and  $v_{\scriptscriptstyle F}$ the Fermi velocity.

## Typical Measurement Configurations (continued)

#### Hall measurement

Hall measurements are an alternative for extracting the mobility and charge carrier density on graphene. In this case,  $V_{SD}$  is applied between the longitudinal contacts, whereas the transversal voltage or Hall voltage,  $V_{HV}$  is measured.  $V_{HV}$  varies with the out-of-plane applied magnetic field, B: due to the Lorentz force that the charge carriers experience, which deflect them toward the transverse contact, an electric field is created and measured by  $V_{HV}$  (see Figure 3a).



**Figure 2:** Scheme of the 4-probe measurement in a Hall bar device, with the corresponding electrical measurement configuration.

The hall mobility  $(\mu_H)$  and charge carrier density  $(n_H)$  are calculated as follows:

$$n_H = \frac{1}{R_H \cdot e}$$

where  $R_{\scriptscriptstyle H}$  is the Hall coefficient:

$$R_H = \frac{dV_H}{dB} \cdot \frac{1}{I_{SD}}$$

Lastly, the mobility can be calculated as:

$$\mu_H = \frac{n_H \cdot e}{R_S}$$

Applications: Photovoltaics, sensors, biosensors, analytics, electronics, dielectrics, optics, semiconductors, graphene research

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